AMENDMENT TO THE CLAIMS

Claim 1 (Currently Amended): An ~~integrated circuit~~apparatus comprising:
an integrated circuit, said integrated circuit including:

a test controller having an instruction register and a test access port finite state machine (TAP FSM), said test controller generates a first global control signal, said global control signal is a packet including a shift signal and a load signal;

at least one logic unit controller;

a single test bus directly coupled between the test controller and the at least one logic unit controller;

at least one design-for-test-feature coupled to the at least one logic unit controller; and

a logic unit coupled to the at least one design-for-test-feature

wherein said test controller encodes and transmits states of said TAP FSM and test signals to said at least one logic unit controller over said single test bus to test said integrated circuit, said logic unit controller generates a ~~first local control~~local shift signal and a ~~second~~ local ~~control~~ load signal from the packet,

wherein said integrated circuit performs tests and generates test signals directly on said integrated circuit.

Claim 2 (Canceled)

Claim 3 (Currently Amended): The ~~integrated circuit~~apparatus of claim 1 wherein the logic unit controller is a deskew controller.

Claim 4 (Currently Amended): The ~~integrated circuit~~apparatus of claim 1 wherein the single test bus is an internal test bus.

Claim 5 (Currently Amended): The ~~integrated circuit~~apparatus of claim ~~4~~ wherein the internal test bus includes n number of lines such that

$$n = a + \log_2 i$$

where n = number of lines, a = number of ancillary transmission bits, and $\log_2 i$ = number of instruction bits.

Claim 6 (Currently Amended): The ~~integrated circuit~~apparatus of claim 5 wherein the number of instruction bits are represented within the content of said instruction register, said instruction register is compliant with IEEE 1149.1.

Claim 7 (Currently Amended): The ~~integrated circuit~~apparatus of claim 5 wherein the ancillary transmission bits include at least one of a clock signal, at least one state of a test access port finite state machine, a security bit, a test data input, and a counter value.

Claim 8 (Currently Amended): The ~~integrated circuit~~apparatus of claim 7 wherein the at least one state of a test access port finite state machine are encoded into three bits.

Claim 9 (Currently Amended): The ~~integrated circuit~~apparatus of claim 7 wherein the at least one state of a test access port finite state machine is allocated into a one-bit test-logic-reset state, a one bit run-test/idle state, and a two-bit residual state.

Claim 10 (Currently Amended): A platform comprising:

a support structure;

a controller disposed on the support structure and coupled to an input device;

at least one memory chip disposed on the support structure and coupled to the controller through a processor bus, said controller generates a first global control signal, said global control signal is a packet including a shift signal and a load signal; and

an integrated circuit having a test controller having an instruction register and a test access port finite state machine (TAP FSM), at least one logic unit controller, a single test bus directly coupled between the test controller and the at least one logic unit controller, at least one design-for-test-feature coupled to the logic unit controller, and a logic unit coupled to the at least one design-for-test-feature, said logic unit controller generates a ~~first~~ local shift~~control~~ signal and a ~~second~~ local ~~control~~ load signal from the packet,

wherein said test controller encodes and transmits states of said TAP FSM and test signals to said at least one logic unit controller over said single test bus to test said platform and said integrated circuit performs and generates test signals directly on said integrated circuit.

Claim 11 (Canceled)

Claim 12 (Previously Presented): The platform of claim 10 wherein at least one of the following is true: the test controller is an integrated test controller; the logic unit controller is a deskew controller; and the single test bus is an internal test bus.

Claim 13 (Original): The platform of claim 12 wherein the internal test bus includes n number of lines such that

$$n = a + \log_2 i$$

where n = number of lines, a = number of ancillary transmission bits, and $\log_2 i$ = number of instruction bits.

Claim 14 (Original): The platform of claim 13 wherein the number of instruction bits are represented within the content of an instruction register that is compliant with IEEE 1149.1.

Claim 15 (Original): The platform of claim 13 wherein the ancillary transmission bits include at least one of a clock signal, at least one state of a test access port finite state machine, a security bit, a test data input, and a counter value.

Claim 16 (Original): The platform of claim 15 wherein the at least one state of a test access port finite state machine are encoded into three bits.

Claim 17 (Original): The platform of claim 15 wherein the at least one state of a test access port finite state machine is allocated into a one bit test-logic-reset state, a one bit run-test/idle state, and a two bit residual state.

Claim 18 (Currently Amended): A method comprising:

generating a test information packet in a test controller of an integrated circuit;

transmitting the test information packet to at least one logic unit controller over a single test bus directly coupled between the test controller and the at least one logic unit controller;

processing the test information packet within the at least one logic unit controller to generate a local shift signal and a local load signal~~test control signals~~;

transmitting the ~~test control~~local shift signals and the local load signal to the at least one design-for-test-feature coupled to the logic unit controller,
wherein said ~~test control~~local shift signals and said local load signal are generated on said integrated circuit to perform tests on said integrated circuit.

Claim 19 (Previously Presented): The method of claim 18 further comprising:

interacting with a logic unit coupled to the at least one design-for-test-feature based on the at least one test control signal.

Claim 20 (Previously Presented): The method of claim 19 wherein transmitting the test information packet to at least one logic unit controller over the single test bus includes transmitting the test information packet over n number of lines such that

$$n = a + \log_2 i$$

where n = number of lines, a = number of ancillary transmission bits, and $\log_2 i$ = number of instruction bits.

Claim 21 (Canceled)

Claim 22 (Previously Presented): The platform of claim 10, wherein a shift signal and a load signal are transmitted in a single packet from said test controller to said at least one logic unit controller.

Claim 23 (Previously Presented): The method of claim 18, wherein a shift signal and a load signal are transmitted in a single packet from said test controller to said at least one logic unit controller on said single test bus.